Comparison Between Simulations and Measurements of Large Signal and Nonlinear Noise Behaviors of MMIC Analog Frequency Divider by Two

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***Abstract*— For the first time, the large signal and nonlinear noise behaviors of an analog frequency divider has been fully simulated and measured: comparisons between predicted and measured results of this circuit are given. The circuit designed is a monolithic microwave integrated circuit (MMIC) X-band 8.2–4.1-GHz analog frequency divider by two. The large signal analysis relies on the open-loop method extended to synchronous systems. The simulation of noise behavior of such a circuit has been performed by means of the nonlinearities conversion matrices and noise generators correlation matrices analysis.**

I. Introduction

NOWADAYS, communication systems require sophisticated frequency generation circuits such as phase-locked loops and frequency synthesizers. Analog frequency dividers offer the possibility of being integrated with other electronic functions in the same GaAs Chip. Moreover, the noise performances are supposed to be better than those of digital ones [1]. Consequently, frequency division is a key function of these circuits [2] and can be performed in a digital or an analog way. To reach high performance, the monolithic microwave integrated circuit (MMIC) technology seems efficient. The aim of this letter is to present the comparison between simulations and measurement of a X-band (8.2–4.1 GHz) analog frequency divider by two, which is the part of frequency generation circuit for a satellite load of telemeasurement. This circuit was processed by using a qualified MESFET 0.7-μm high-power technology. However, to simulate such a circuit, CAD tools can present an important deficit, mainly in noise simulation. So, we have developed specific design methods to calculate the large-signal regime [3] and the noise performance of these potentially unstable circuits. To our knowledge, it is the first-reported analysis of noise performances of a frequency divider. For each kind of analysis, some comparisons between simulated and measured results are presented.

II. Design and Large Signal Analysis of the Analog Divider by Two

The working principle of the analog divider relies on a closed loop in which the output signal at the divided frequency is fed back and mixed with the external signal to produce a lower sideband at the output frequency, which will be filtered and amplified. In addition, this closed-loop circuit may oscillate at the divided frequency without external generator. The block diagram of such a circuit is shown in Fig. 1. A phase relation must exist between the injection signal and the output signal in order to get a synchronous stable regime. The divider, whose electrical scheme is presented in Fig. 2, is composed of an input buffer amplifier providing the required power and matching to the working of a second active stage, which behaves as a frequency divider at $f_0/2 = 4.1$ GHz. The large-signal design of this circuit is based on the open-loop method extended to synchronous systems detailed in [3]. The large-signal model of the transistor is presented in Fig. 3 [4]. Without any injected signal, the analog frequency divider by two acts as a free-running oscillator working at the frequency of 4.1 GHz. This way, the output power versus the output frequency is measured and simulated for different input powers, equal to -1 and 4 dBm. The results are presented in Fig. 4. A good accuracy is also obtained between the simulated and experimental results. Note that a flat power of 8 dBm on about the whole synchronized band is obtained for a -1-dBm input power. A 12% synchronized bandwidth around the central frequency for an input power of 4 dBm is obtained.

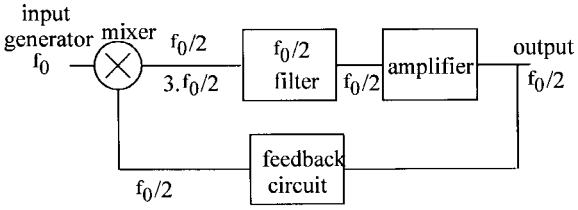

Fig. 1. Diagram of frequency divider by two.

III. Nonlinear Noise Analysis of the Analog Divider by Two

The noise behavior of the divider is perturbed by internal noise sources (additive noise) and by the amplitude and phase noise spectra of the synchronizing generator. The simulation technique we have implemented allows to take into account both noise sources. This simulation method is based on conversion matrix formalism [5], [6]: it consists of representing the active device nonlinearities by their conversion matrices. Moreover, in this analysis, noise generators are depicted by

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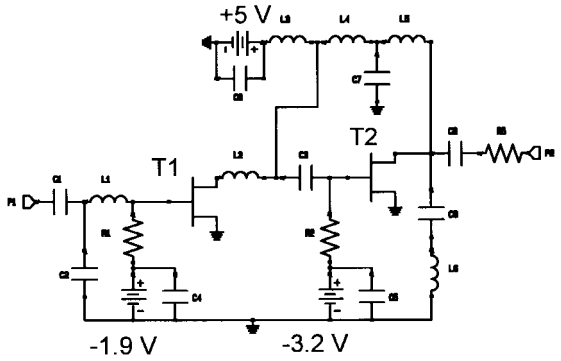

Fig. 2. Electrical scheme of the frequency divider.

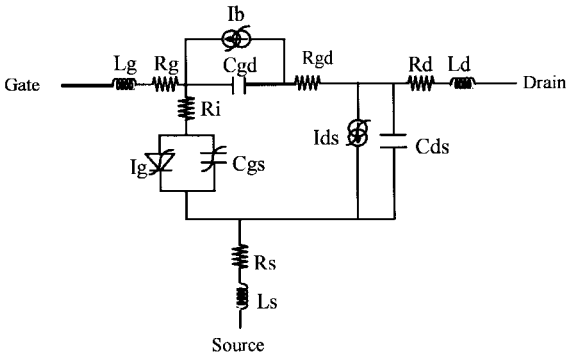

Fig. 3. Nonlinear model of the transistor.

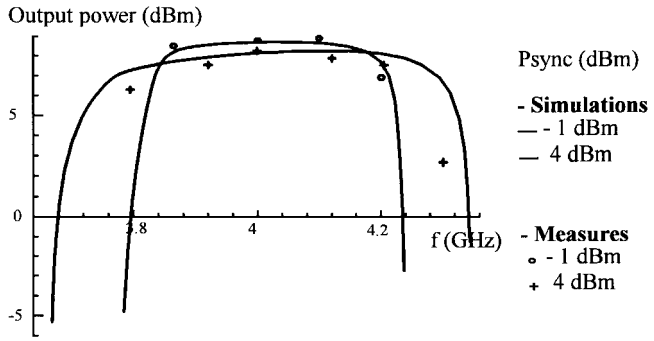

Fig. 4. Output power versus synchronized bandwidth.

their correlation matrices. To perform such an analysis, the divider in large signal steady-state regime must be perfectly known. Moreover, the low-frequency noise sources of the transistor and the noise spectrum of synchronizing generator must be measured and introduced into CAD tool to calculate phase noise spectrum. The transistor low-frequency noise model used in the simulation is the classical model, with only one voltage-equivalent noise generator at the input of the transistor. Its spectral density has a k/f law with a constant $k = 9.58\text{e} - 10$. To operate in the frequency divider regime, the divider has been synchronized by an external source at frequency f_0, which varies in the locking band [7.6–8.4 GHz] and presents the phase noise spectrum density of Fig. 5. For a synchronized input power of 2 dBm, the output phase noise spectrum has been simulated and measured in the whole synchronized bandwidth. For the simulation,

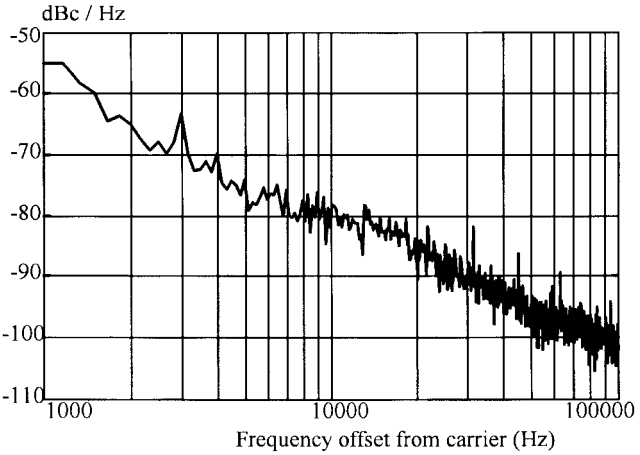

Fig. 5. Phase noise spectrum of the synchronizing oscillator.

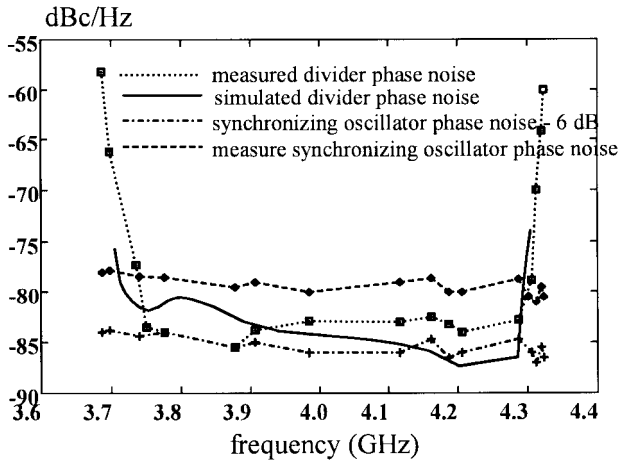

Fig. 6. Simulated and measured phase noise spectra against the locking band.

both divider low-frequency noise and synchronizing oscillator phase noise spectrum have been taken into account. These phase noise spectrum results at 10 kHz offset from the carrier versus synchronized frequency are given in Fig. 6. The input phase noise minus the reduction of 6 dB due to the division row is also reported in this figure. Note that the copy of this spectrum is not being kept constant in the whole locking range, as is obtained with a simple model [7]. At the edges of the synchronized band, the noise increases due to unstability of the divider. To the best of our knowledge, these are the first simulations and measurements carried out over the whole synchronization band by taking into account the complete circuit.

IV. Conclusion

This letter presents the comparison between simulations and measurements of large signal and noise behavior of a MMIC X-band 8.2–4.1-GHz analog frequency divider by two. This device has been designed with large-signal analysis using the open-loop method extended to the synchronous circuits to permit us obtaining 12% synchronized bandwidth for an input power of 2 dBm and a flat output of 9 dBm. For the first time

published, the phase noise spectrum was compared with good accuracy between simulated and measured ones.

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